

TEKTRONIX
PG 502

TEKTRONIX®

PG 502

250 MHz

PULSE GENERATOR

FOR REFERENCE PURPOSES ONLY

INSTRUCTION MANUAL

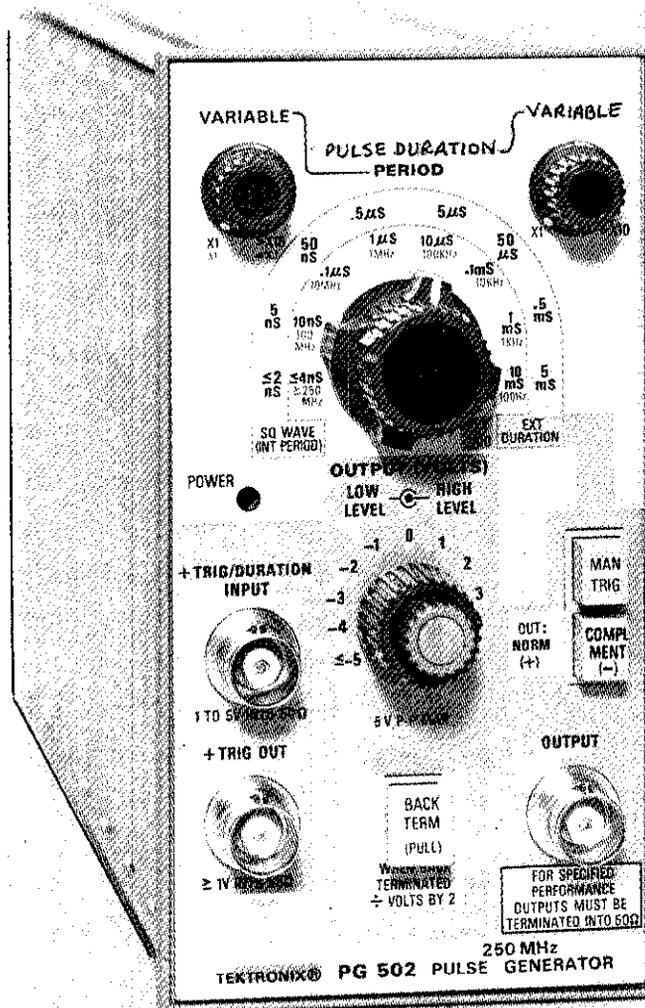
Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97005

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Serial Number _____

TABLE OF CONTENTS

SECTION 1	OPERATING INSTRUCTIONS	Page
	Introduction	1-1
	Instrument Description	1-1
	Installation and Removal	1-1
	Operating Considerations	1-2
	Output Terminations and Connections	1-2
	Maintaining Pulse Fidelity	1-2
	Impedance Matching	1-2
	Risetime Measurements In Linear Systems	1-4
	Variable Pulse Delay	1-4
	Operating Modes	1-5
	Period and Duration Selection	1-5
	Output Levels	1-5
	External Trigger	1-5
	External Duration	1-5
	Functions Available at Rear Connector	1-6
	Definitions Of Pulse Characteristics	1-6
	Specifications	1-8
	Performance Conditions	1-8
SECTION 2	THEORY OF OPERATION	2-1
	Introduction	2-1
	Low Frequency Period Generator	2-1
	4ns Period Generator	2-1
	External Trigger Duration Buffer	2-1
	Manual Trigger Multivibrator	2-2
	Period and Trigger Out Buffers	2-2
	Trigger Shaper	2-2
	Duration Generator	2-2
	Output Buffer	2-2
	Output Driver	2-2
	Output Amplifier	2-2
	Output Level Programmer	2-2
	Power Supply	2-3
SECTION 3	SERVICE INFORMATION	
	Symbols and Reference Designators	3-1
	Rear Interface Connector Assignments	3-2
	Electrical Parts List	3-3
	Internal Adjustment Procedure	
	Timing Board Parts Location Grid	
	Front Panel Controls and Connectors	
	Block Diagram	
	Output Board Parts Location Grid	
	Generators and Trigger Schematic	
	Output Schematic	
	Switch Details and Power Supply Schematic	
	Mechanical Parts List	
	Exploded View	
	Accessories and Repackaging	



OPERATING INSTRUCTIONS

INTRODUCTION

Instrument Description

The PG 502 is a 250 MHz general purpose pulse generator for use in the TM 500 series power modules. Major capabilities of this instrument include high repetition rate, narrow pulse width, fast risetime, and independent pulse top and bottom level controls. Front panel controls provide manual trigger, square wave output, and complementary pulse output for high duty factors.

A selectable 50 Ω back termination in the pulse output circuitry is also provided. All other inputs and outputs are internally terminated in 50 Ω .

Triggers preceding the output pulse are available at the front panel. The pulse output may also be externally triggered.

The front panel is color coded for easy reference to controls and their associated functions. Orange denotes pulse duration controls and settings; green, triggering functions; and yellow is used for an operating caution note. Alpha-numeric digits done in red are the frequency equivalents for the pulse period settings.

Installation and Removal

The PG 502 is calibrated and ready for use when received. It operates in any compartment of a TM 500 series power module. See the power module instruction manual for line voltage requirements and power module operation. Fig. 1-1 shows the installation and removal procedure. Check that the PG 502 is fully inserted in the power module. Pull the power switch on the power module. The POWER light on the PG 502 front panel should now be on. Refer to the Controls and Adjustments foldout page in Section 3 of this manual, for a complete description of the front panel controls.

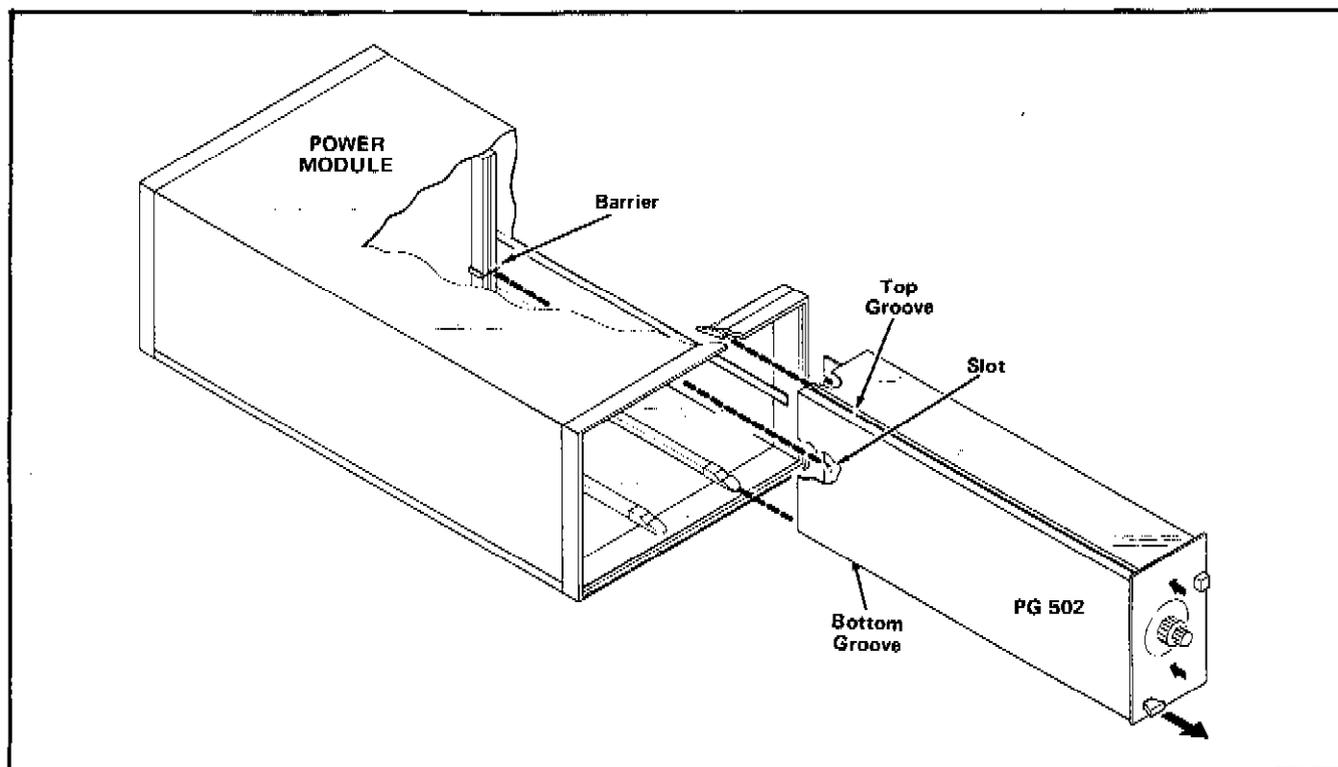


Fig. 1-1. PG 502 Installation and Removal.

OPERATING CONSIDERATIONS

Output Terminations and Connections

The output of the PG 502 operates as a 100 mA current source. It is designed to operate into an external 50 Ω load. An unterminated or improperly terminated output causes aberrations on the output pulse (see Impedance Matching). Loads less than 50 Ω reduce the pulse amplitude. Loads greater than 50 Ω increase the amplitude. An external 50 Ω load also provides a DC return path for the output current.

A selectable 50 Ω back termination is provided (pull the button labeled BACK TERM (PULL) on the front panel). The back termination also helps to absorb reflections. The output voltage is divided by two when using the back termination. The back termination provides the DC return path for the output when driving high impedance or capacitively-coupled loads. If the output of the PG 502 drives a high impedance load using the back termination, the output voltage is limited to approximately ±5 V.

A DC current in the 50 Ω output load causes the output pulse to be offset. Do not apply voltages greater than plus or minus 5 V to the output of the PG 502. If the load has a DC voltage across it greater than the maximum allowed, connect a blocking capacitor in series with the OUTPUT connector and the load. Use the back termination to provide a DC return path for the output current. Make certain the time constant of the capacitor and the load is large enough to maintain pulse flatness. The output circuitry of the PG 502 is fully protected against any voltage transients in the output resulting from passive loads.

Under certain conditions, it is possible to operate the PG 502 into a high impedance load without using the internal termination. Pulse amplitudes up to about 18 V (−9 V to +9 V) can be obtained in this manner with load impedances in excess of 180 Ω. The PG 502 is not specified when operating in this mode. To use the instrument in this manner, view the output with an oscilloscope while adjusting the OUTPUT (VOLTS) controls for the desired waveform.

Maintaining Pulse Fidelity

Due to the extremely fast pulse risetimes obtained from the PG 502, special consideration must be given to preservation of pulse fidelity. Even at low repetition rates, 1 GHz frequency components are present in the output waveform. Use high quality coaxial cables, attenuators, and terminations.

RG 58 type coaxial cable and typical BNC connectors exhibit impedance tolerances which may cause visible

reflections. For maximum fidelity, use the special three foot long 50 Ω coaxial cable with special BNC connectors supplied as a standard accessory (Tektronix Part No. 012-0482-00). Use the internal back termination whenever possible.

When signal comparison measurements or time difference determinations are made, the two signals from the test device should travel through coaxial cables with identical loss and time delay characteristics.

Make certain the attenuators and terminations used can safely handle the maximum PG 502 power output of 0.5 Watts.

When making connections that are not in a 50 Ω environment, keep all lead lengths short, 1/4 inch or less. Accessory filters to increase risetimes and reduce the need for high quality attenuators and terminations are available. See your Tektronix Representative for more information.

Impedance Matching

A mismatch, or different impedance in a transmission line, generates a reflection back along the line to the source. The amplitude and polarity of the reflection are determined by the load impedance in relation to the characteristic impedance of the cable. If the load impedance is higher than the characteristic impedance of the line, the reflection will be of the same polarity as the applied signal. If it is lower, the reflection will be of opposite polarity. These reflections add or subtract from the amplitude of the incident pulse causing distortion and irregular pulse shapes.

A simple resistive minimum attenuation impedance-matching network that can be used to match the PG 502 output into relatively low impedances is shown in Fig. 1-2. To match impedances with the illustrated network, the following conditions must exist:

$$\frac{(R_1 + Z_2) R_2}{R_1 + Z_2 + R_2} \text{ must equal } Z_1$$

and

$$R_1 + \frac{Z_1 R_2}{Z_1 + R_2} \text{ must equal } Z_2.$$

Therefore:

$$R_1 R_2 = Z_1 Z_2, \text{ and } R_1 Z_1 = R_2 (Z_2 - Z_1)$$

or

$$R_1 = \sqrt{Z_2 (Z_2 - Z_1)}$$

and

$$R_2 = Z_1 \sqrt{\frac{Z_2}{Z_2 - Z_1}}$$

For example; to match a 50 Ω system to a 125 Ω system, Z_1 equals 50 Ω and Z_2 equals 125 Ω.

Therefore:

$$R_1 = \sqrt{125(125 - 50)} = 96.8 \text{ ohms,}$$

and

$$R_2 = 50 \sqrt{\frac{125}{125 - 50}} = 64.6 \text{ ohms.}$$

Though the network in Fig. 1-2 provides minimum attenuation, for a purely resistive impedance-matching device, the attenuation as seen from one does not equal that seen from the other end. A signal (E_1), applied from the lower impedance source, encounters a voltage attenuation (A_1) which is greater than 1 and less than 2, as follows:

$$A_1 = \frac{E_1}{E_2} = \frac{R_1}{Z_2} + 1$$

A signal (E_2) applied from the higher impedance source (Z_2) encounters a greater voltage attenuation (A_2) which is greater than 1 and less than $2(Z_2/Z_1)$:

$$A_2 = \frac{E_2}{E_1} = \frac{R_1}{R_2} + \frac{R_1}{Z_1} + 1.$$

In the example of matching 50 Ω to 125 Ω,

$$A_1 = \frac{96.8}{125} + 1 = 1.77$$

and

$$A_2 = \frac{96.8}{64.6} + \frac{96.8}{50} + 1 = 4.43.$$

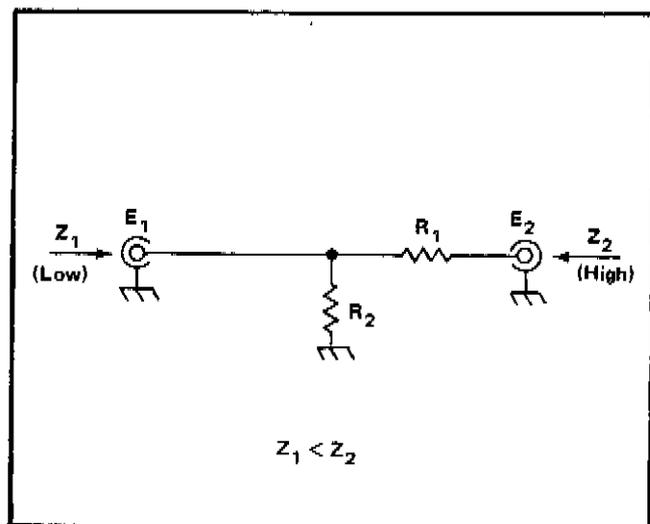


Fig. 1-2. Impedance matching network that provides minimum attenuation.

The illustrated network can be modified to provide different attenuation ratios by adding another resistor (less than R_1) between Z_1 and the junction of R_1 and R_2 .

When constructing such a device, the environment surrounding the components should also be designed to provide smooth transition between the impedances. Acceptable performance can be obtained with discrete components using short lead lengths; however, a full coaxial environment is preferred.

The characteristic impedance of a coaxial device is determined by the ratio between the outside diameter of the inner conductor to the inside diameter of the outer conductor expressed as:

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \log_{10} D/d.$$

The relative dielectric constant is ϵ ($\epsilon_{air} = 1$), D is the inside diameter of the outer conductor and d is the diameter of the inner conductor.

Further information on attenuator design may be found in Reference Data For Radio Engineers, Fifth Edition, Howard W. Sams & Co. Inc., New York, N.Y., Chapt. 10, or other suitable reference work.

Consider carefully the effects of impedance mismatches or discontinuities in transmission lines and terminations. Short lengths of wire exhibit inductance causing pulse aberrations. Use 50 Ω environments or, if this is impossible, keep all lead lengths as short as possible (1/4 inch or shorter).

Operating Instructions—PG 502

If the PG 502 is driving the 1 MΩ capacitively-shunted vertical input of an oscilloscope, connect a 50 Ω termination to the oscilloscope input. Connect the coaxial cable from the PG 502 to a 50 Ω 10X attenuator, and connect the attenuator to the termination. The attenuator isolates the input capacity, providing an improved termination for the cable. Another method is to back terminate the PG 502 by pulling the BACK TERM (PULL) pushbutton on the front panel, and connecting the coaxial cable to the oscilloscope input through a 50 Ω termination.

Risetime Measurements in Linear Systems

Consider the rise and falltime of associated equipment when measuring the rise or falltime of a linear device. If the risetime of the device under test is at least ten times slower than the combined risetimes of the PG 502, the monitoring oscilloscope, and associated cables, the error introduced will not exceed 1%, and usually may be ignored. If the rise or falltime of the test device is less than ten times slower than the combined risetimes of the testing system, determine the actual risetime of the device under test by using the following formula:

$$R_t = \sqrt{R_1^2 + R_2^2 + R_3^2 + \dots}$$

R_t equals the overall rise or falltime of the entire measurement system and $R_1, R_2, R_3,$ etc. are the risetimes or falltimes of the individual components comprising the system.

Variable Pulse Delay

Variable pulse delays may be obtained using another PG 502, or other suitable pulse generator. For example, using two PG 502s, push the COMPLEMENT button and, using an oscilloscope, set the OUTPUT (VOLTS) LOW LEVEL control on the delay generator for 0 V. Set the HIGH LEVEL control for +1 V. Some fine tuning of the output levels of this generator may be necessary to achieve 250 MHz operation. Connect the OUTPUT from the delay generator to the +TRIG/DURATION INPUT connector on the output generator. Take the pulse output from the OUTPUT connection on the output generator, and the trigger from the + TRIG OUT connector on the delay generator.

The PERIOD controls on the delay generator now set the period of the output waveform, and the DURATION controls set the delay. The output pulse duration and voltage levels are set by the appropriate controls on the output generator. See Fig. 1-3.

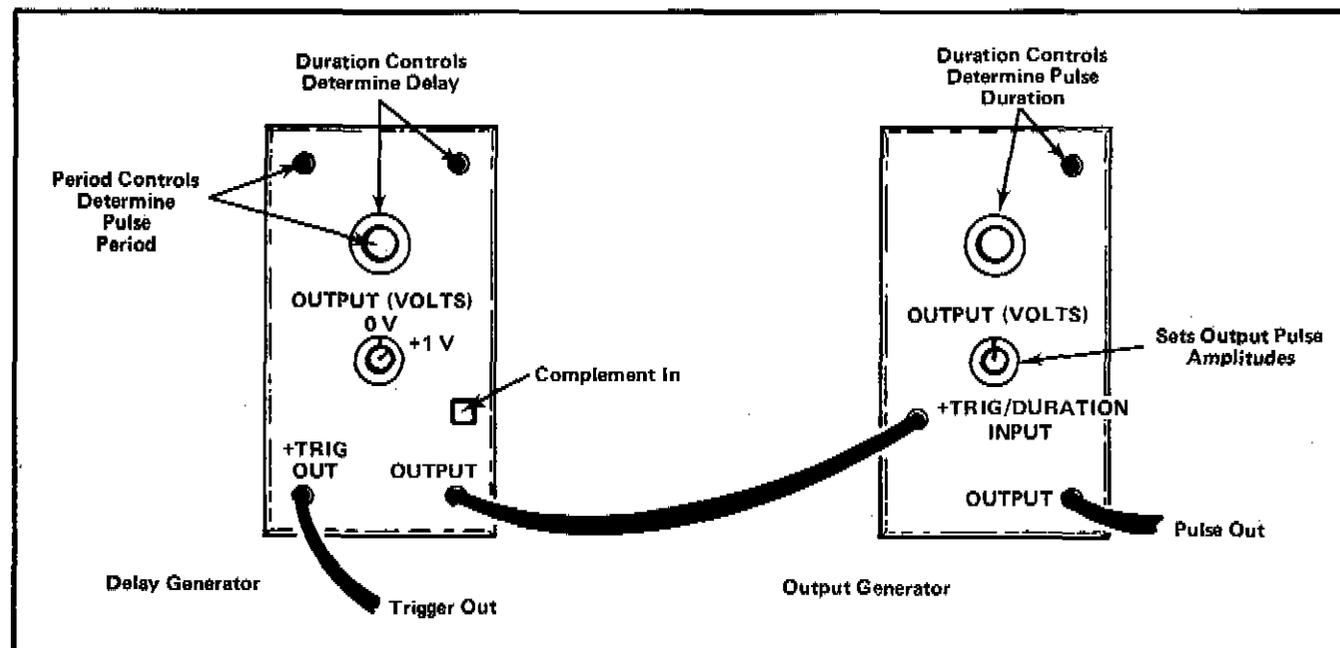


Fig. 1-3. Setup using two PG 502s to obtain Variable Pulse Delay.

OPERATING MODES

Period and Duration Selection

The period generator free runs at the rate set by the PERIOD selector and the PERIOD VARIABLE control in all modes except SQ WAVE and EXT DURATION. The duration of the output pulse is set by the PULSE DURATION selector and its associated PULSE DURATION VARIABLE control. The PERIOD and PULSE DURATION selectors are mechanically coupled, so the duty factor cannot exceed 50% with the VARIABLE controls in the X1 positions. Under most circumstances, duty factors far in excess of the specified 50% may be obtained in the NORM mode using the VARIABLE controls. Excessive duty factor is indicated by any of the following pulse abnormalities: (1) pulse output period in multiples of the trigger output period, and (2) alternate pulses with durations less than the pulse duration setting.

Duty factors approaching 100% may be obtained by switching to the complement mode. Set the PULSE DURATION control for a pulse width equal to the desired pulse off time and push the front panel COMPLEMENT (—) pushbutton.

In the square wave mode, the duration is automatically set to approximately 50% of the period setting.

Output Levels

The output amplitude and offset are selected by independent pulse HIGH LEVEL and pulse LOW LEVEL controls. Use the front panel voltage calibration marks when the load resistance is $50\ \Omega$, and the back termination is not used. The output voltage is one half of the voltage indicated by the dial calibration when the back termination is used. The OUTPUT (VOLTS) controls are interlocked so that it is impossible to set the HIGH LEVEL control more negative than the low level. It is also impossible to set the controls for more than about 5.5 V P-P output amplitude into $50\ \Omega$. Pulse amplitude always equals the pulse high level minus the pulse low level. Offset may be the high level or the low level, whichever is used as the baseline reference level. The flexibility of this method of controlling the output amplitude and offset is useful in certain applications such as logic testing, i.e., either the high or low level can be varied without disturbing the other.

Use of the normal complement function allows interchanging the pulse on-off times without varying the voltage levels.

External Trigger

The period generator is disabled when the PERIOD selector is in the EXT TRIG position. An external positive-going signal applied to the TRIG/DURATION IN connector, triggers the duration generator. The pulse duration of the output pulse varies with the front-panel pulse DURATION selector and VARIABLE control. The period of the output waveform is the period of the triggering signal. See Fig. 1-4. The external trigger signal must remain above the recognition threshold for at least 2 ns. It must also remain below the reset threshold for at least 2 ns to reset the generator for the next trigger.

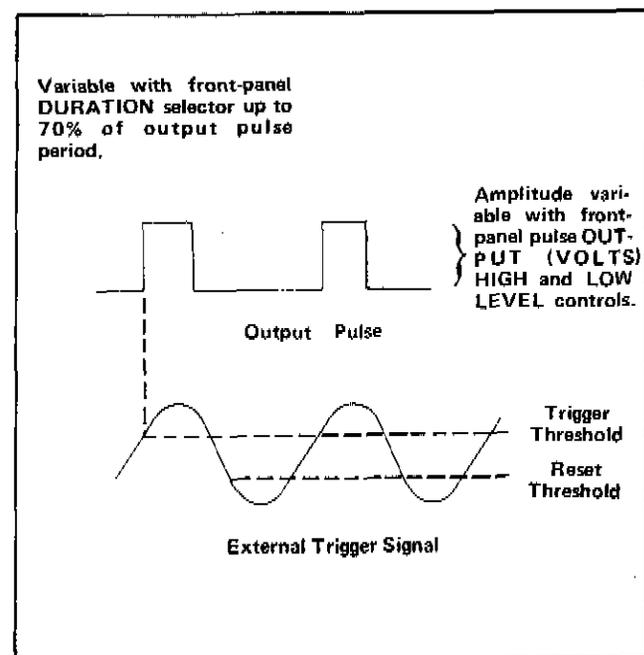


Fig. 1-4. External trigger signal and output pulse in EXT TRIG mode.

A manual trigger is available for single pulse operation. Disconnect any external trigger input when not in use.

External Duration

The period generator and duration generator are disabled when the DURATION selector is in the EXT DURATION position. A voltage exceeding the recognition level applied to the TRIG/DURATION INPUT connector will activate the output of the PG 502. The period and duration of the output will depend on the period and duration of the externally-applied voltage. See Fig. 1-5. When operating in this mode, the output of the PG 502 is activated as long as the MAN TRIG pushbutton is depressed.

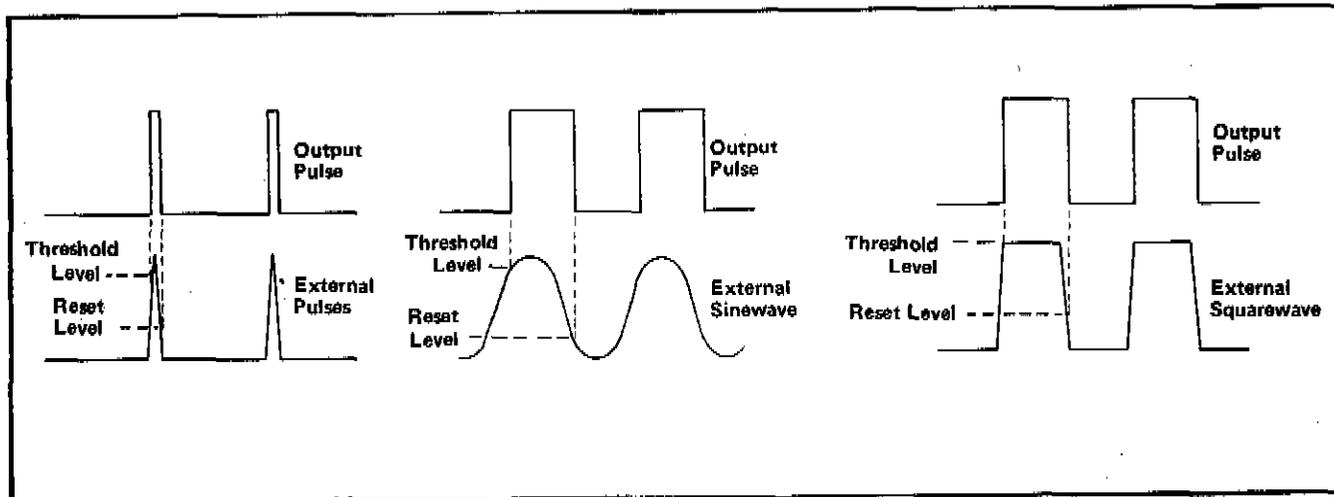


Fig. 1-5. External gating signals and output pulses in EXT DURATION mode.

FUNCTIONS AVAILABLE AT REAR CONNECTOR

Refer to the rear connector assignment illustration in the Service Section at the rear of this manual for suggested pin assignments. These connections are not factory wired.

To obtain a trigger out signal complementary to the front panel trigger out pulse, connect one end of a coaxial cable to the pads on the Timing Board marked Internal Trig Out. Connect the other end to appropriate pins as shown in the illustration. Connections made to the Internal Trig Out pads do not interfere with the front panel + TRIG OUT signals. A one-half volt signal into 50Ω is available at the Internal Trig Out pads.

To obtain the + TRIG OUT signal at the rear interface connector, disconnect the coaxial cable from the front panel + TRIG OUT connector and the coaxial connector labeled Trig Out on the Timing Board. Replace this cable with another 50Ω cable about ten inches long, with a similar coaxial connector on one end. Solder the other end to the holes located as shown in the illustration.

To obtain Trigger/Duration input capabilities at the rear interface connector, remove the coaxial cable from the front panel connector and the coaxial connector on the Timing Board. Use a new piece of coax about ten inches long with suitable connection. Solder the free end of this cable to the rear interface pads located as shown in the illustration.

Remember, when planning to use the rear interface connectors, pulse fidelity may be disturbed due to the impedance mismatch the signals are subjected to in passing through the connectors.

A slot between pins 23 and 24 on the rear connector identifies the PG 502 as a member of the signal source family. A barrier may be inserted in the corresponding position of the power module jack to prevent other than signal source plug-ins from being used in that compartment. This protects the plug-in should specialized connections be made to that compartment. Consult the *Building A System* section of the power module manual for further information.

DEFINITIONS OF PULSE CHARACTERISTICS

The following is a glossary of common pulse characteristics used in this manual. They are illustrated in Fig. 1-6.

Amplitude. The maximum absolute peak value of a pulse measured from the baseline regardless of sign, and

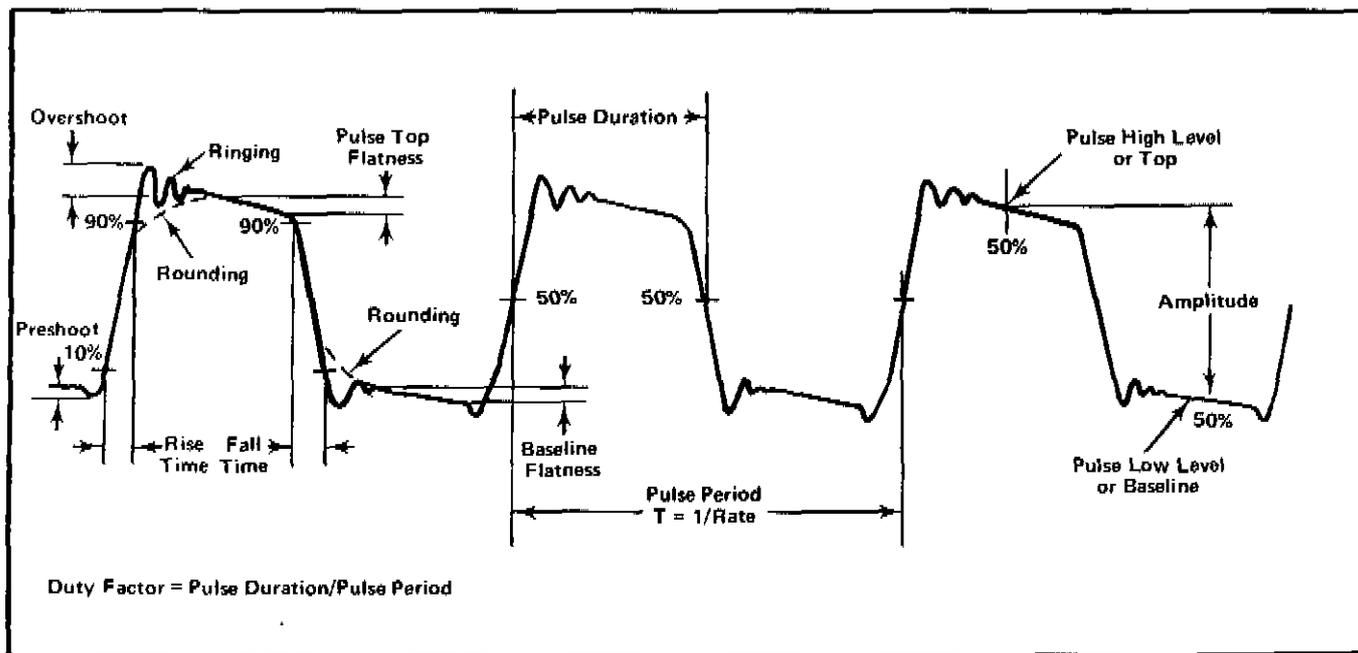


Fig. 1-6. Pulse characteristics.

excluding unwanted aberrations or overshoot. Measurement points are at 50% of the pulse duration time (pulse high level) and on the baseline (pulse low level) at 50% of the off time (the pulse period minus the pulse duration).

Aberrations. Unwanted deviations or excursions in the pulse shape from an ideal square corner and flat top, i.e., overshoot, undershoot or rounding, ringing, and tilt or slope.

Baseline. The quiescent DC voltage reference level of the pulse waveform.

Complementary Pulse. Normal pulse with high and low levels interchanged. Pulse on-time becomes pulse off-time.

Duty Factor. Sometimes referred to as duty cycle. The ratio of pulse duration to period, or the product of pulse duration and pulse repetition rate. Duty factor in % = Duration/Period X 100.

Falltime. The time interval, at the pulse trailing edge, for the pulse amplitude to fall from the 90% amplitude level to the 10% amplitude level.

Flatness. The absence of long term variations to the pulse top; excluding overshoot, ringing or pulse rounding. Sometimes referred to as tilt or slope.

High Level. The most positive value of a pulse, regardless of unwanted aberrations or overshoot, measured at a point that is located at 50% of the pulse duration.

Low Level. The most negative value of a pulse, regardless of unwanted aberrations or overshoot, measured at a point that is at 50% of the off time.

Offset. A DC potential of either polarity applied to the waveform to bias the baseline to an amplitude other than zero.

Overshoot. The short term pulse excursion (or transient) above the pulse top or below the baseline, which is simultaneous to the leading or trailing edge of the pulse.

Period. The time interval for a full pulse cycle, inverse of frequency or repetition rate, or the interval between corresponding pulse amplitudes of two consecutive undelayed or delayed pulses. Generally measured between the 50% amplitude levels of two consecutive pulses.

Preshoot. A transient excursion that precedes the step function. It may be of the same or opposite polarity as the pulse.

Pulse Duration. The time interval between the leading and trailing edge of a pulse at which the instantaneous amplitude reaches 50% of the peak pulse amplitude.

Operating Instructions—PG 502

Polarity. The direction from the baseline of the pulse excursion, either positive-going (+) or negative-going (-).

Ringing. Periodic aberrations that dampen in time, following the overshoot.

Risetime. The time interval, at the step function leading edge, for the pulse to rise from the 10% to the 90% amplitude levels.

Rounding or Undershoot. The rounding of the pulse corners at the edges of a step function.

Tilt or Slope. A distortion of an otherwise flat-topped pulse, characterized by either a decline or a rise of the pulse top. (see Flatness).

SPECIFICATIONS

Performance Conditions

The electrical characteristics are valid only if the PG 502 is calibrated at an ambient temperature between +20°C and +30°C and operated between 0°C and +50°C. Specifications apply only with 50 Ω output load impedances.

PERIOD:

Range: ≤ 4 ns, 10 ns to 10 ms in decade steps. Variable control allows overlap on all ranges and extends period to ≥ 100 ms.

Accuracy: 5% in calibrated positions, from 10 ns to 1 ms, 15% on 10 ms range.

Jitter: $\leq 0.1\% + 50$ ps.

TRIGGER IN:

Amplitude: Trigger threshold ≤ 1 V, reset threshold ≥ 0.1 V maximum input 5 V DC + peak AC. Derate to 2 V P-P @ 250 MHz.

TRIGGER OUT:

Amplitude: ≥ 1 V into 50 Ω.

DELAY:

Fixed: $\cong 10$ ns from trigger out to pulse out.

DURATION:

Range: ≤ 2 ns, 5 ns to 5 ms in decade steps. Variable control allows overlap on all ranges, and extends duration to ≥ 50 ms.

Accuracy: 5% from 5 ns to .5 ms, 15% of 5 ms range, with both period and duration variables in calibrated positions. Duration may vary not more than 3% + 0.5 ns for any duty factor less than 50%.

Duty Factor: At least 50% in normal pulse mode; 100% in complement mode. Minimum off time 2 ns.

External Duration: Leading edge threshold level ≤ 1 V, trailing edge reset level ≥ 0.1 V. Maximum input, 5 V, DC + peak AC. Derate to 2 V P-P @ 250 MHz.

Jitter: $\leq 0.1\% + 50$ ps.

OUTPUT:

Amplitude: Pulse high and low levels independently adjustable over a -5 V to +5 V range, with pulse amplitude limited between ≥ 0.5 V and ≤ 5 V. Complement switch inverts pulse between same two selected voltage levels. Front panel selectable 50 Ω internal back termination divides output levels by two.

Risetime: ≤ 1 ns.

Falltime: ≤ 1 ns.

Aberrations: $< +$ and -5% at 5 V P-P amplitude, except negative transition aberrations may exceed 5% for durations less than 5 ns.

Pulse Top Flatness: $\geq 2\%$, beginning 10 ns after transition.

INTERNAL POWER DISSIPATION: 14 watts maximum.

should be $\leq 20\%$.

THEORY OF OPERATION

Introduction

Use the block diagram in the foldout pages of this manual, along with the detailed schematic diagrams, and the following discussion to understand the operation of the PG 502. Integrated circuits U150, U180, and U260 use emitter-coupled logic (ECL). This logic is non-saturating for high speed operation. The high level is approximately 4.4 V above ground and the low level is 3.6 V.

Low Frequency Period Generator

U150B operates as an astable multivibrator for settings of the PERIOD switch of 10 ns and longer. See Fig. 2-1 for a simplified diagram of the Low Frequency Period Generator. When any input of the OR/NOR gate is high, the

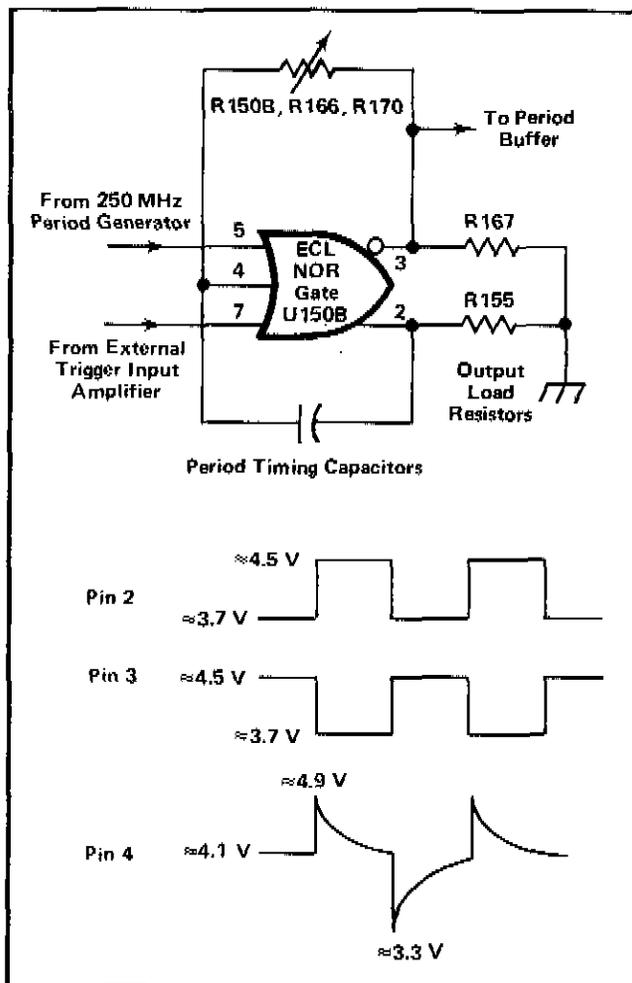


Fig. 2-1. Simplified Low Frequency Period Generator with associated waveforms.

output (pin 2) is high. The switched timing capacitances are connected from pin 2 to pin 4 of U150B. The capacitors are switched by the period range switch. R150B, the PERIOD VARIABLE control, varies the resistance in the negative feedback loop.

To start the period cycle, assume pin 2 of U150B goes high. This positive step is coupled through the Period timing capacitor to pin 4. Pin 3 goes low. As the timing capacitor discharges through the PERIOD VARIABLE resistance, the voltage at pin 4 decays at a rate determined by the timing capacitor and the PERIOD VARIABLE resistance. When the switching level (approximately 4 V) is reached, pin 2 goes low and pin 3 goes high. The negative step at pin 2 is coupled through the timing capacitor, and appears at pin 4. The capacitor now charges through the PERIOD VARIABLE resistance until the switching level is reached, and the period cycle repeats.

A slight offset current is applied through the Symmetry Adj control to compensate for the input current in U150B. This current controls the symmetry of the trigger output pulse. Output to the trigger buffer is taken from pin 3.

4 ns Period Generator

In the ≤ 4 ns position of the PERIOD selector, the feedback for U150B is disconnected via contact 3 of S150A. Contact 13F of S150A opens enabling U150A. U150A operates exactly as U150B, in the Low Frequency Period Generator. The associated circuitry is optimized for high speed operation.

External Trigger Duration Buffer

When the PG 502 is operated in the EXT TRIG or EXT DURATION mode, U150B operates as an externally-triggered Schmitt multivibrator with positive feedback through R158 and contact 12F of S150A. Q125 and Q130 serve as a high gain comparator-amplifier for external trigger-duration input signals. The base of Q130 is set by R135 and R136 at about 0.5 V. A trigger-duration input signal greater than about 0.5 V causes a negative-going output step at the collector of Q125. This step is transmitted through the strip line to the Low Frequency Period Generator. CR130 provides temperature compensation. CR122, CR123, CR125, and R122 protect the input against excessive voltages.

Theory of Operation—PG 502

Manual Trigger Multivibrator

This circuit, an emitter-coupled Schmitt multivibrator, eliminates false triggers due to contact bounce in the MAN TRIG front panel switch. The PULSE PERIOD switch must be in the EXT TRIG position for this circuit to operate. When the switch is pushed, the base of Q100 is connected to the +15 V supply through R100. This turns Q100 off and Q110 on. The collector of Q110 goes positive, causing a positive-going trigger at the base of Q125 in the External Trigger Input circuitry. Q106 provides positive feedback to hold the collector of Q110 positive during the contact bounce interval.

Period and Trigger Out Buffers

U180A, an OR/NOR gate, serves as a buffer to drive Q185 and Q190. These transistors operate as an emitter-coupled amplifier. The collector of Q185 drives the front panel + TRIG OUT BNC connector. The collector of Q190 is connected to the Internal Trig Out connection on the Output circuit board.

Trigger Shaper

The output from the Trigger Buffer is also fed to OR/NOR gate U180B. Q210, Q220, Q230, and Q240 serve as emitter-coupled trigger amplifiers. These amplifiers supply a fast rise current step to the trigger differentiator, Q245. When troubleshooting this circuit, any capacitance greater than about 2 pF connected between TP1 and ground renders this circuit inoperative.

A current step applied to the emitter of Q245 produces a voltage step at the collector. The collector-to-base feedback capacitance of the transistor causes this step to appear at the base, and subsequently the emitter. The base and emitter voltages decay toward their initial values. The decay time is set by R248, R249, and the transistor capacitance.

When pin 13 is in the high state, during square wave or external duration operation, the trigger shaper is disabled, and the external duration pulse is fed directly to the Output Buffer through R266.

Duration Generator

The positive-going trigger pulse, applied to pin 10 of U260A, causes pin 14 to go low and pin 15 high. Pin 15 is held high by positive feedback through R262. The low at the base of Q270 turns Q270 off. The emitter of Q270 goes negative at a rate allowed by the timing capacitor and the variable timing current source, Q290. As the emitter of Q270 goes negative, it pulls pin 12 of U260A negative through Q288. When pin 12 reaches the switching threshold (approximately +4 V), pin 14 goes positive and the mono-

stable duration generator resets until the next positive-going trigger pulse repeats the process. Output is taken from U260A, pin 15.

Output Buffer

This OR/NOR gate, U260B, shapes the signal fed to the Output board. The timing waveform at pin 3 of U260B, is essentially the waveform seen at the output of the PG 502. In the square wave mode, or external duration mode, the waveform at pin 7 controls the output of U260B, (the trigger having been disabled at U180B). The push-pull timing waveform is applied to the bases of Q320 and Q335, connected as an emitter-coupled amplifier. Their collectors are connected to the bases of a second emitter-coupled amplifier, Q350 and Q354, through zener diodes, VR320 and VR335. These diodes change the voltage to a more appropriate level for the following circuitry.

Output Driver

U360 is the output driver amplifier. It also performs the normal complement pulse switching function. Q390 is a variable output current source that tracks the output current to provide a constant ratio of driver current to output current. Q406 supplies one-half the value of current supplied by Q390, to provide a reference level for U400. This reference level lies halfway between the high and low voltage levels at the output of U360.

Output Amplifier

U400 switches up to 100 mA between either the external load (terminating resistance), or R442 and R443. Q470 is the variable output current source. The amplitude of the output pulse is proportional to the current supplied by Q470.

Output Level Programmer

Q504 and Q508 supply up to ± 100 mA of current to the output load. L446, L447, L450, L451, R447 and R450 decouple the source from the output pulse. The offset level of the output pulse is proportional to the current supplied by Q504 and Q508.

The output programming circuitry takes input from the pulse HIGH LEVEL and LOW LEVEL controls to provide proper control current to the amplitude (Q390, Q470) and offset (Q504, Q508) current sources.

When the amplifier output, U400 pin 2, is in the high state (amplifier off), the output voltage is proportional to the offset current. Turning the HIGH LEVEL control clockwise causes pin 3 of U480A to go negative. The

emitters of Q516 and Q520 also go negative due to the action of U480A, an operational amplifier. Conduction is increased in Q520 and decreased in Q516. Current flow is increased in Q504 and decreased in Q508. This action causes an absolute magnitude current increase in the load resistance (collectors of Q504 and Q508 move in the positive direction). This current change is sensed through R502 and R508 and fed back to pin 2 of U480A, causing a stable condition at its input. The output current (pulse high level) is proportional to the setting of the HIGH LEVEL control.

The output amplifier is on when the pulse output is in the low state. The output voltage is proportional to the sum of the offset current and the switched output current.

Manual control of the pulse low level occurs by varying the voltage at pin 5 of U480B with the front panel LOW LEVEL control. Turning the LOW LEVEL control CW causes pin 7 of U480B to go more positive. This increases the current through Q470 and consequently the pulse amplitude. The output high level is unchanged as the low level goes lower. Pin 6 of U480B, connected to the emitter of Q470 through R493, also goes more positive, until the voltage between pins 5 and 6 of U480B is zero.

If the pulse high level is raised, more current must flow in the output amplifier to keep the pulse low level at the same voltage. When the collectors of Q504 and Q508 go positive, their emitters go negative. This change is coupled through R495 to pin 6 of U480B. Pin 7 of U480B goes positive, increasing current flow through the Output Amplifier, and effectively increasing pulse amplitude. The pulse low level is unaffected by adjustment of the pulse HIGH LEVEL control. The Low Level Bal, internal adjustment, is provided to optimize the tracking of the output level programming circuitry.

Diodes CR445, VR445, CR446, CR448, CR449, and VR449 protect U400 against voltage reflections from reactive loads.

Power Supply

U640 is a precision voltage regulator for the +5 V supply. R645 sets the value of the output voltage however, it is adjusted for accuracy of the +15 V supply, as this is the most critical voltage in the PG 502. Internal reference voltage from U640 is available at pin 6. Operating voltage at pin 12 is pre-regulated by VR616, for reduced ripple. 11.5 V DC is applied to the collectors of Q650. The +5 V is

taken from the emitter. If the current to the PG 502 is increased, pin 4 of U640, connected to the emitter of Q650, goes negative. This causes pin 10 to go positive, increasing current flow through Q650, and restoring the voltage to its preset value. Should the current supplied increase excessively, the voltage drop across R650 causes Q650 to decrease conduction through internal action in U640, limiting the current to a safe value.

Q606 and Q610 serve as a comparator for the +15 V supply. If the +15 V supply goes negative, due to increased load, Q606 will decrease conduction. Its collector will go positive increasing conduction in Q600. This will increase current flow in emitter follower Q612, which is connected to the series pass transistor in the main frame. The series pass transistor will increase current available to the load, and the voltage is restored to the correct value. R615 sets the maximum current available from the supply. If the +15 V is shorted, Q600 saturates with its collector approximately 3 V (due to VR600) below the unregulated supply. This drop is reduced, by the base emitter drops of Q612, and the series pass transistor in the main frame, to about 1.6 V across R615. This drop limits the maximum current available from the supply. F600 additionally protects the components from overcurrent.

The -20 V supply is connected to the base of Q660. If the -20 V goes more negative, conduction increases in Q660. This reduces conduction in Q670, and Q674 connected to the base of the series pass transistor in the main frame. The series pass transistor reduces conduction, restoring the -20 V to its preset level. Current is limited through R676. If the supply is shorted, Q660 reduces conduction, saturating Q670 with its collector approximately 3 V from the unregulated voltage. The drop across the base emitter junction of Q674, and the series pass transistor in the main frame, sets the voltage across R676, at which the series pass transistor limits the current available. Fuse F670 further protects components from abnormal currents. CR675 prevents the -20 V supply from going positive with respect to ground.

Additional protection for the PG 502 is provided by Q626, and its associated components. If the +15 V supply goes to about 17 V, Q620 conducts, causing the gate of Q626 to move in the positive direction. When the gate of Q626 is about 1 V positive with respect to the cathode, the diode conducts, shorting the +15 V, +5 V and the -20 V supplies together. If the -20 V supply goes several volts more negative, Q632 conducts, causing the same action in Q626, and shorting the +15 V, and -20 V and +5 supplies.

If the fault remains, the current limits in the +15 V, -20 V and +5 V supplies protect the circuitry. Should the current limits fail, fuses F600 and F670 will open.